WHAT IS CLAIMED IS:

1. A method of operating a programmable logic integrated circuit comprising:

loading an initial value in a count register of a watchdog timer circuit of the programmable logic integrated circuit;

clocking the count register to advance the count register to a next value with each clock;

periodically reloading the count register with the initial value;

when the stored count value held in the count register of the watchdog timer circuit reaches a final value, asserting a triggered signal output; and

upon receiving the triggered signal output in a reset logic block of the programmable logic integrated circuit, causing reloading of configuration data from an external source into the programmable logic integrated circuit.

2. The method of claim 1 wherein the external source is a nonvolatile memory.

3. The method of claim 1 wherein the external source is a serial EPROM.

4. The method of claim 1 wherein the final value causes an overflow condition for the count register of the watchdog timer circuit.

5. The method of claim 1 wherein the watchdog timer circuit increments the stored count value at each clock pulse.

6. The method of claim 1 wherein the watchdog timer circuit decrements the stored count value at each clock pulse.

7. The method of claim 1 wherein periodically reloading the count register comprises:

writing a magic value into a reload register of the watchdog timer circuit; and

when the magic value is received in the reload register, resetting the count register of the watchdog timer circuit to the initial value.

8. The method of claim 1 wherein periodically reloading the count register comprises:

writing a first magic value into a reload register of the watchdog timer circuit;

when the first magic value is received in the reload register, reloading the count register of the watchdog timer circuit to the initial value; and

after the first magic value is received in the reload register, permitting a subsequent reload of the count register when a second magic value is written into reload register.

9. The method of claim 8 further comprising:

continually reloading the count register to the initial value by writing the first and second magic values to the reload register in sequence, alternately.

10. The method of claim 1 further comprising:

using the configuration data to configure an embedded processor portion and a programmable logic portion of the programmable logic integrated circuit.

11. The method of claim 1 wherein to avoid asserting the triggered signal output, a periodic reload of the watchdog timer circuit should be performed during a time period it takes the watchdog timer circuit to count from the initial value to the final value.

12. The method of claim 11 wherein the period is less than about two minutes.

13. The method of claim 11 wherein the time period depends on clock frequency used to clock the watchdog timer circuit.

14. The method of claim 1 wherein the initial value is 0 and the final value is a maximum count value permitted by the count register.

15. The method of claim 1 wherein the count register comprises 32 bits.

16. A method of designing a programmable logic integrated circuit comprising:

taking a first layout of a programmable logic integrated circuit;

stretching the first layout using an edge of the first layout so the first layout has a stretched section;

taking a second layout of an embedded processor stripe for a programmable logic integrated circuit, wherein the embedded processor stripe comprises a watchdog timer circuit;

incorporating the second layout into stretched section of the first layout; and

coupling signal lines of the first layout to signal lines of the second layout.

17. The method of claim 16 further comprising:

fabricating the programmable logic integrated circuit using a combination of the first and second layouts.

18. A programmable logic integrated circuit designed according to the method recited in claim 16.

19. A method comprising:

designing a layout of an embedded processor stripe to be incorporated into a programmable logic integrated circuit; and

including in the layout a watchdog timer circuit.

20. The method of claim 19 further comprising:

including signal lines in the layout of the embedded processor stripe to be coupled to signal lines of a programmable logic portion of the programmable logic integrated circuit.

21. The method of claim 19 wherein the layout is designed to be positioned at an edge of the programmable logic integrated circuit.

22. A circuit comprising:

a programmable logic integrated circuit comprising an embedded processor portion and a programmable logic portion, wherein the embedded processor portion includes a watchdog timer circuit; and

an external configuration source integrated circuit, coupled to the programmable logic integrated circuit, storing configuration information for the programmable logic integrated circuit, wherein when the watchdog timer circuit asserts a triggered signal output due to not

reloading the watchdog timer circuit within a timeout period, configuration data is loaded from the external configuration source into the programmable logic integrated circuit.

23. The circuit of claim 22 wherein the external configuration source is a nonvolatile memory.

24. The circuit of claim 22 wherein the watchdog timer circuit is reloaded by periodically loading a reload register of the watchdog timer with one or more magic values.

25. The circuit of claim 22 wherein a configuration of the programmable logic portion of the programmable logic integrated circuit is held using volatile memory cells.

26. The circuit of claim 25 wherein the volatile memory cells are SRAM cells.

27. The circuit of claim 22 wherein configuration data from the external configuration source is used to configure the embedded processor portion and programmable logic portion of the programmable logic integrated circuit.

28. The circuit of claim 22 wherein the configuration is transferred serially from the external configuration source to the programmable logic integrated circuit.

29. The circuit of claim 22 wherein the watchdog timer circuit is not reloaded due to a software failure occurring within the embedded processor portion of the programmable logic integrated circuit.

30. The circuit of claim 22 wherein the watchdog circuit is not reloaded due to a power supply problem.

31. A programmable logic integrated circuit comprising:

a programmable logic portion of the integrated circuit comprising a plurality of logic array blocks, configurable to perform user logic, wherein the logic array blocks are arranged in rows and columns; and

an embedded processor portion of the integrated circuit, coupled to the programmable logic portion, comprising a watchdog timer circuit which is triggered if a count

register of the watchdog timer circuit is permitted to count to a final value before the count register is reloaded.

32. The programmable logic integrated circuit of claim 31 wherein triggering of the watchdog timer circuit is avoided when the watchdog timer circuit is periodically reloaded, before a timeout period, by writing a magic value to a reload register.

33. The programmable logic integrated circuit of claim 32 wherein the timeout period is a time it takes for the watchdog timer circuit to count from an initial value to the final value.

34. The programmable logic integrated circuit of claim 31 wherein the plurality of logic array blocks are configured by programming SRAM memory cells.

35. The programmable logic integrated circuit of claim 31 wherein the plurality of logic array blocks are configured by programming volatile memory cells.

36. The programmable logic integrated circuit of claim 31 wherein the watchdog timer circuit comprises a reload register and a control register.

37. The programmable logic integrated circuit of claim 31 wherein each logic array block comprises a look-up table circuit.

38. The programmable logic integrated circuit of claim 31 wherein after the watchdog timer circuit is triggered, a reset circuit of the programmable logic integrated circuit effects loading of configuration data from an external source to reconfigure the programmable logic and embedded processor position of integrated circuit.

39. The programmable logic integrated circuit of claim 31 wherein the embedded processor portion further comprises a central processing unit and an embedded processor memory block, coupled together using a first bus.

40. The programmable logic integrated circuit of claim 39 wherein the watchdog timer circuit is also coupled to the first bus.

41. The programmable logic integrated circuit of claim 39 wherein the embedded processor further comprises a second bus, through which the memory block is coupled to the programmable logic portion of the integrated circuit.

42. The programmable logic integrated circuit of claim 39 wherein the external source is a Flash memory, EPROM memory, nonvolatile memory, or serial memory.

43. The programmable logic integrated circuit of claim 38 wherein the configuration data is transferred to the programmable logic integrated circuit by using a serial stream of bits.

44. A method of operating a programmable logic integrated circuit comprising:

clocking a watchdog timer circuit to advance a count register of the watchdog timer circuit;

loading a first magic value into a reload register of the watchdog timer circuit, which resets the count register to an initial value;

after loading the first magic value, loading a second magic value into the reload register, which causes the count register to reset the initial value; and

after loading the first magic value into the reload register, loading a value other than the second magic value into the reload register, which causes the watchdog timer circuit to generate a triggered signal.

45. The method of claim 44 further comprising:

receiving the triggered signal in a reset logic block of the integrated circuit, which causes a reloading of configuration data from an external source into the integrated circuit.

46. The method of claim 45 wherein the configuration data is used to configure an embedded processor portion and a programmable logic portion of the integrated circuit.

47. The method of claim 45 wherein the watchdog timer circuit is located in an embedded processor portion and the reset logic block is located in a programmable logic portion of the integrated circuit.

48. The method of claim 44 further comprising:

allowing the count register of the watchdog timer to advance to a final value before the first or second magic values are loaded, which causes the watchdog timer circuit to generate the triggered signal.

49. The method of claim 44 wherein the initial value is 0.

50. The method of claim 44 wherein the initial value is a value other than 0.

51. The method of claim 44 wherein the first magic value is different from the second magic value.

52. The method of claim 48 wherein the final value is user-selectable.

53. The method of claim 48 wherein the final value is the maximum count permitted by the count register.

54. The method of claim 44 wherein in a debug mode, the count register does not advance.